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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
LUU, CHUONG A	

ART UNIT	PAPER NUMBER
2818	

DATE MAILED: 01/12/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	10/780,529	JAN ET AL.
	Examiner	Art Unit
	Chuong A. Luu	2818

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *03* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *28 October 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-23,36-48 and 50-64* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-23,36-48 and 50-64* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *11/14/2005*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

PRIOR ART REJECTIONS

Statutory Basis

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

The Rejections

Claims 1-2, 5-6, 8-9, 12-14, 16-17, 19, 21-23, 36-37, 41-43, 45-48, 50-54, 58-60 and 62-64 are rejected under 35 U.S.C. 102(e) as being anticipated by Hembree et al. (U.S. 6,380,555 B1).

Hembree discloses a bumped semiconductor component

(1); (48); (53) forming a barrier layer (78) comprising a barrier layer material on the substrate (54) and on the exposed portion of the metal layer (66);

forming a conductive bump (58) comprising a conductive bump material on the barrier layer (78) wherein the barrier layer (78) is between the conductive bump (58) and the substrate (54) and wherein the conductive bump (58) is laterally offset and laterally separated from the exposed portion of the metal layer (66) (see Figure 2B);

after forming the conductive bump (58), removing the barrier layer (78) from the exposed portion of the metal layer (66) while maintaining a portion of the barrier layer (78) between the conductive bump (58) and the substrate (54) so that the portion of the barrier layer maintained between the conductive bump and the substrate is laterally offset and laterally separated from the exposed metal layer in the direction parallel to the surface of the substrate and so that the exposed portion of the metal layer is free of the barrier layer material (see Figure 2B);

(2); (54) wherein the substrate comprises an integrated circuit substrate (see Figure 2B);

(5) wherein the metal layer, the barrier layer, and the conductive bump all comprise different materials (see Figure 2B);

(6) further comprising: before forming the conductive bump, forming a conductive under bump metallurgy layer on the barrier layer; and before removing the barrier layer, removing the conductive under bump metallurgy layer from the barrier layer opposite the metal layer while maintaining a portion of the conductive under bump metallurgy layer between the conductive bump and the substrate so that the portion of the barrier layer maintained between the conductive bump and the substrate is laterally offset and laterally separated from the exposed metal layer in the direction parallel to the surface of the substrate and so that the exposed portion of the metal layer is free of the conductive under bump metallurgy layer (see Figure 2B);

(8) wherein the conductive under bump metallurgy layer and the barrier layer comprise different materials (see Figure 2B);

(9) further comprising: before forming the conductive bump, forming a second barrier layer on the under bump metallurgy layer wherein the second barrier layer and the under bump metallurgy layer comprise different materials and wherein the second barrier layer is between the conductive bump and the conductive under bump metallurgy layer (see Figure 2B);

(12) wherein forming the second barrier layer comprises selectively forming the second barrier layer on a portion of the under bump metallurgy layer wherein the second barrier layer is offset from the metal layer (see Figure 2B);

(13) wherein forming the conductive bump comprises selectively forming the conductive bump on the second barrier layer offset from the metal layer (see Figure 2B);

(14) wherein selectively forming the second barrier layer and selectively forming the conductive bump comprise selectively forming the second barrier layer and the conductive bump using a same mask (see Figure 2B);

(16) wherein forming the conductive bump comprises selectively plating the bump on the barrier layer offset from the metal layer (see Figure 2B);

(17) wherein the integrated circuit substrate includes an input/output pad thereon, wherein the barrier layer is formed on the substrate including the metal layer and the input/output pad, and wherein the conductive bump is formed on the barrier layer opposite the input/output pad (see Figure 2B);

(19) wherein the substrate includes an input/output pad thereon, wherein the barrier layer is formed on the substrate including the metal layer and the input/output

pad, and wherein after removing the barrier layer from the metal layer, the conductive bump is electrically coupled to the input/output pad (see Figure 2B);

(21) wherein the conductive bump is formed on the barrier layer opposite the input/output pad (see Figure 2B);

(22) wherein the conductive bump is offset from the input/output pad (see Figure 2B);

(23) further comprising: after removing the barrier layer from the metal layer, bonding a second substrate to the conductive bump (see Figure 2B);

(37) wherein the electronic device comprises an integrated circuit device, and wherein the substrate comprises an integrated circuit substrate (see Figure 2B);

(41) further comprising: forming a conductive under bump metallurgy layer between the barrier layer and the conductive bump (see Figure 2B);

(42) further comprising: bonding a second substrate bonded to the conductive bump (see Figure 2B);

(43); (60) wherein the integrated circuit substrate includes an input/output pad thereon and wherein the barrier layer and the conductive bump are electrically connected to the input/output pad (see Figure 2B);

(45) wherein the conductive bump is on the barrier layer opposite the input/output pad (see Figure 2B);

(46); (62) wherein the conductive bump is offset from the input/output pad (see Figure 2B);

(47); (58) further comprising: an under bump metallurgy layer between the barrier layer and the conductive bump wherein the under bump metallurgy layer and the barrier layer comprise different materials (see Figure 2B);

(59) further comprising: bonding a second substrate bonded to the conducive bump (see Figure 2B);

(63) wherein the conductive bump is laterally offset from the input/output pad in a direction parallel to the surface of the substrate (see Figure 2B);

(64) further comprising: an under bump metallurgy layer between the barrier layer and the conductive bump wherein the under bump metallurgy layer and the barrier layer comprise different material (see Figure 2B).

PRIOR ART REJECTIONS

Statutory Basis

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The Rejections

Claims 3-4, 7, 10-11, 15, 18, 20, 38-40, 44, 55-57 and 61 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hembree et al. (U.S. 6,380,555 B1)

Hembree discloses the claimed invention except for specific materials. It would have been obvious to one having ordinary skill in the art at the time the invention was made to select specific material to be apply to fabricate a semiconductor device, since it has been held to be within the general skill of a worker in the art to select a known material on the basis of its suitability for the intended use as a matter of obvious design choice. In re Leshin, 125 USPQ 416.

Response to Arguments

Applicant's arguments, see remarks, filed 10/28/2005, with respect to the rejection(s) of claim(s) 1-23 and 36-48 under U.S. 6,475,896 have been fully considered and are persuasive. Therefore, the rejection has been withdrawn. However, upon further consideration, a new ground(s) of rejection is made in view of Hembree et al. (U.S. 6,380,555 B1).

Applicant argues that Hashimoto fails to teach or suggest a metal layer being free of a conductive bump material, or free of a barrier layer material as recited in claim 1. However, Hembree discloses a bumped semiconductor component with metal layer is exposed after etching the barrier layer (78) (see Figure 2B).

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP

§ 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Chuong A. Luu whose telephone number is (571) 272-1902. The examiner can normally be reached on M-F (6:15-2:45).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David C. Nelms can be reached on (571) 272-1787. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Chuong Anh Luu
Patent Examiner
January 06, 2006